Plastic Shottky Barriers Fabricated by a Line Patterning Technology

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Plastic Shottky barriers were fabricated using poly(3,4-ethylenedioxythiophene) doped with poly(4-styrenesulfonate) (PEDOT:PSS) and aluminum as the p-type semiconductor and the metal, respectively, by a facile line-patterning technology in which multiple-line-patterning was utilized for the designed patterns. Based on the measurements of current–voltage and capacitance–voltage characteristics, various electrical parameters of the Shottky barriers were extracted. As a result, the barrier height, work function of the PEDOT:PSS and rectification ratio were 0.78, 4.8 eV and 1.6×10^2, respectively.

Polymer electronic devices have been attracted great attentions since their promising applications for such as organic light-emitting diodes,[1] field-effect transistors,[2–7] and Shottky barrier diodes.[8–11]

Fabrication methods are crucially important for the electronic devices from a viewpoint of cost performance which makes the "ubiquitous" or wide use of them easier. Recently, a line-patterning technology has been developed for fabrication of plastic electronic devices.[12–15] The conventional line patterning technology includes three main steps,[12] i.e., i) design and printing of a pattern; ii) coating on the printed substrate with a functional materials solution; iii) removal of the reverse-printed toner. Although the conventional line patterning technology greatly simplifies the fabrication processes of electronic devices compared with the photoresister lithography, it should be extended further in order to be suitable for more complicated patterns of plastic electronic devices.

Herein, we suggest a multiple-line-patterning method in which the three steps from i) to iii) could be repeated, which easily results in more complicated patterns of the plastic electronic devices. We verify the efficiency of the multiprinting method by fabrication of a Shottky barrier consisting of conductive polymer/metal.

The conductive polymer poly(3,4-ethylenedioxythiophene) doped with poly(4-styrenesulfonate) (PEDOT:PSS) and aluminum were used as a p-type semiconductor and a metal, respectively, for the Shottky barrier. Transparency film of poly(ethyleneterephthalate) (PET) and gold were used as a substrate and another contact metal, respectively.

The typical fabrication procedure of the PEDOT:PSS/Al Shottky barrier is as follows: The first pattern was printed on the PET film by using a commercial laser printer. Subsequently, PEDOT:PSS layer was formed on the patterned PET film by a bar-coating of the corresponding aqueous solution. Then, the printer toner was removed by ultrasonication in toluene. In this stage, top-viewed area of the Shottky barrier was determined. It is also noted that the procedure till this stage is the same three steps of the conventional line patterning technology. The second pattern was printed on the PEDOT:PSS-coated PET film and gold layer was deposited in vacuum, then the toner was removed by ultrasonication. Similarly the third pattern was printed for the vacuum deposition of aluminum. Finally, the PEDOT:PSS/Al Shottky barrier was fabricated by removing the toner. The patterned image and schematic structure of the PEDOT:PSS/Al Shottky barrier fabricated on the PET film are shown in Figure 1.

The electric characteristics of thus-fabricated PEDOT:PSS/Al Shottky barrier was analyzed by using a picoammeter (6487 Keithley) and a LCR meter (3532-50 Hioki). The typical current–voltage characteristics of the Shottky barrier was shown in Figure 2. The Shottky barrier height, work function of the PEDOT:PSS and depletion width were calculated with the current–voltage and capacitance–voltage characteristics curves according to the well-known theoretic equations (see Supporting Information).[16,17] As a result, the barrier height, work function of the PEDOT:PSS and rectification ratio are 0.78, 4.8 eV and 1.6×10^2, respectively. The parameters slightly vary depending on the batches.

Liang et al. previously reported PEDOT:PSS/Al Shottky diode fabricated on heavily doped silicon wafer by combination of spin-coating and vacuum deposition techniques.[11] The Shottky barrier height, work function and rectification ratio are 0.97, 5.16 eV and 1.3×10^4, respectively,[11] calculated according to a modified model.

Therefore, the present Shottky barrier and work function of PEDOT:PSS, i.e., 0.78 and 4.8 eV are well comparable with those reported by Liang et al.[11] The rectification ratio, however,

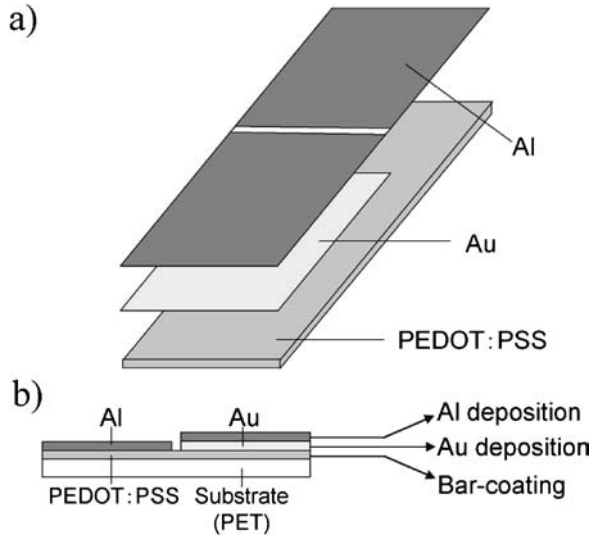

Figure 1. Schematic illustrations of the multiple-line-patterning method. a) Consequently patterned layers and b) cross section of the layers.

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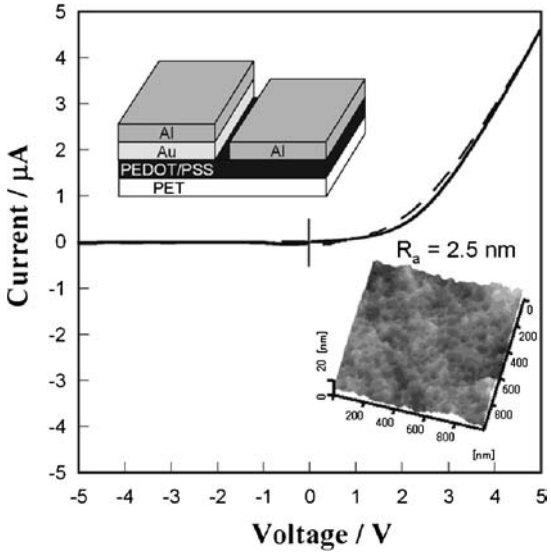

Figure 2. Current–voltage characteristics of the PETOD:PSS/Al Shottky barrier. Insets: The structure of the barrier (top) and AFM image of surface of the PEDOT:PSS layer (bottom).

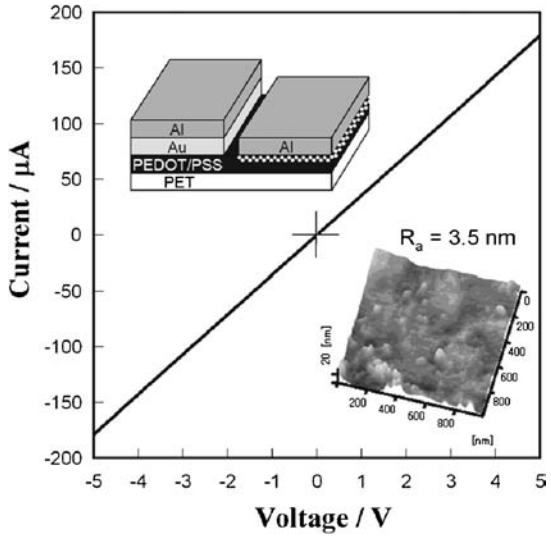

Figure 3. Current–voltage characteristics of the PETOD:PSS/Al ohmic contact. Insets: The structure of the contact (top) and AFM image of surface of the PEDOT:PSS layer (bottom).

are lower by two orders of magnitude than the value reported by Liang et al.[11] It should be noted that our parameters were calculated based on different model from that used by Liang et al.[11] The present patterning method should be optimized further in terms of the diode performance.

We have preliminarily investigated influence of interface between the PEDOT:PSS and the Al layers on the Shottky barrier in terms of roughness of the PEDOT:PSS layer. The difference of the roughness was also induced by the multiple-line-patterning method. Typically, the coated PEDOT:PSS surface was completely covered with the print-toner and then removed by ultrasonication in toluene. We determined the roughness of PEDOT:PSS layer by an atomic force microscopy. Finally, Al was deposited on the PEDOT:PSS layer with higher roughness (3.5 nm). As shown in Figure 3, the contact between the PEDOT:PSS and Al layers exhibited electrically ohmic behavior, while clear Shottky barrier was observed when the roughness is 2.5 nm, as mentioned above. The experimental results suggest that the semiconductor/metal interface crucially influences on the formation of the Shottky barrier, especially in the case of plastic electronic devices fabricated by a wet processing. It is not ruled out that the additional printing/toner-removing treatment also possibly influences the barrier formation.

In conclusion, we suggested a multiple-line-patterning method and verified the efficiency of the multiple-line-patterning method by fabrication of a Shottky barrier consisting of conductive polymer PEDOT:PSS and metal Al. Based on the measurements of current–voltage and capacitance–voltage characteristics, various electrical parameters of the Shottky barriers were extracted. As a result, the barrier height, work function of the PEDOT:PSS and rectification ratio were 0.78, 4.8 eV, and 1.6×10^2, respectively. The preliminary results showed that roughness of interface between PEDOT:PSS and Al layers may crucially influence the formation of the Shottky barrier.

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